Description

The PJ71 series is a set of three-terminal low power high voltage regulators implemented in CMOS technology. They allow input voltages as high as 24V. They are available with several fixed output voltages ranging from 3.0V to 5.0V. Because of the low power dissipation, PJ71 series are widely used in a variety of equipment such as audio device, video device, communication device and so on.

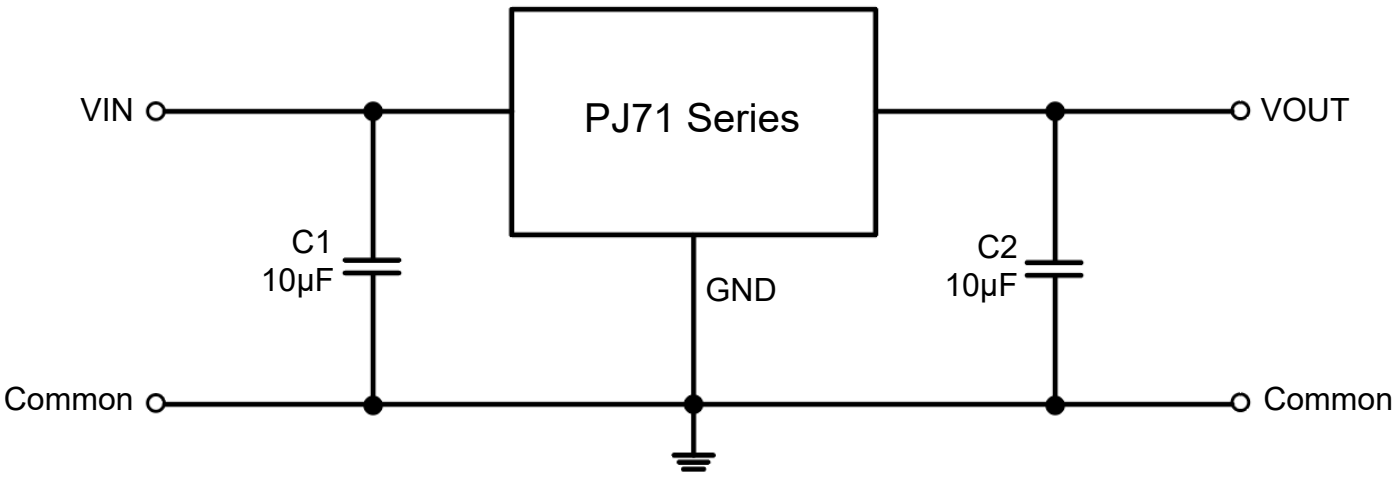
Features

- Low Quiescent Current: 4uA
- High Input Voltage Rating: Up to 24V
- Output Current: 30mA(Typ.)
- Low Dropout : 100mV(Typ.) @ 1mA
- Fixed Output Voltages: 3.0V,3.3V,3.6V,4.4V,5.0V
- Low Power Consumption
- Available Packages: SOT-23、SOT-23-3、SOT-89

Applications

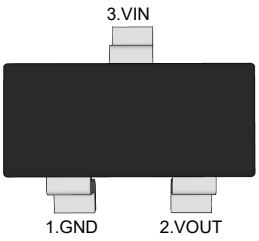
- Battery-Powered Equipment
- Communication Equipment
- Audio/Video Equipment

Typical Application Circuit



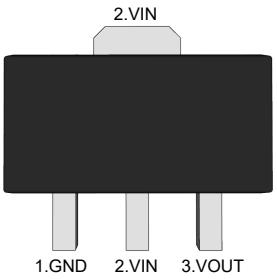
Pin Distribution

SOT-23



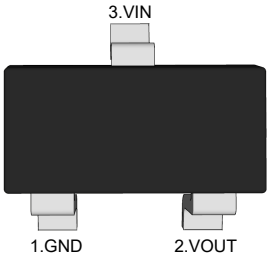
(Top View)

SOT-89



(Top View)

SOT-23-3



(Top View)

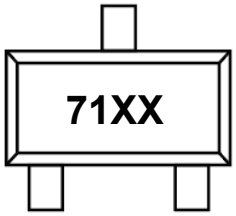
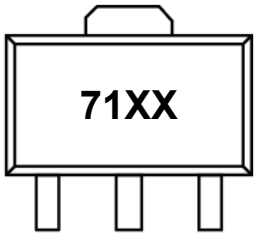
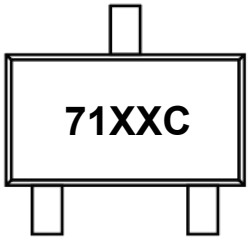
Functional Pin Description

Pin Name	Pin Function
GND	Ground
VOUT	Output Voltage
VIN	Power Input Voltage

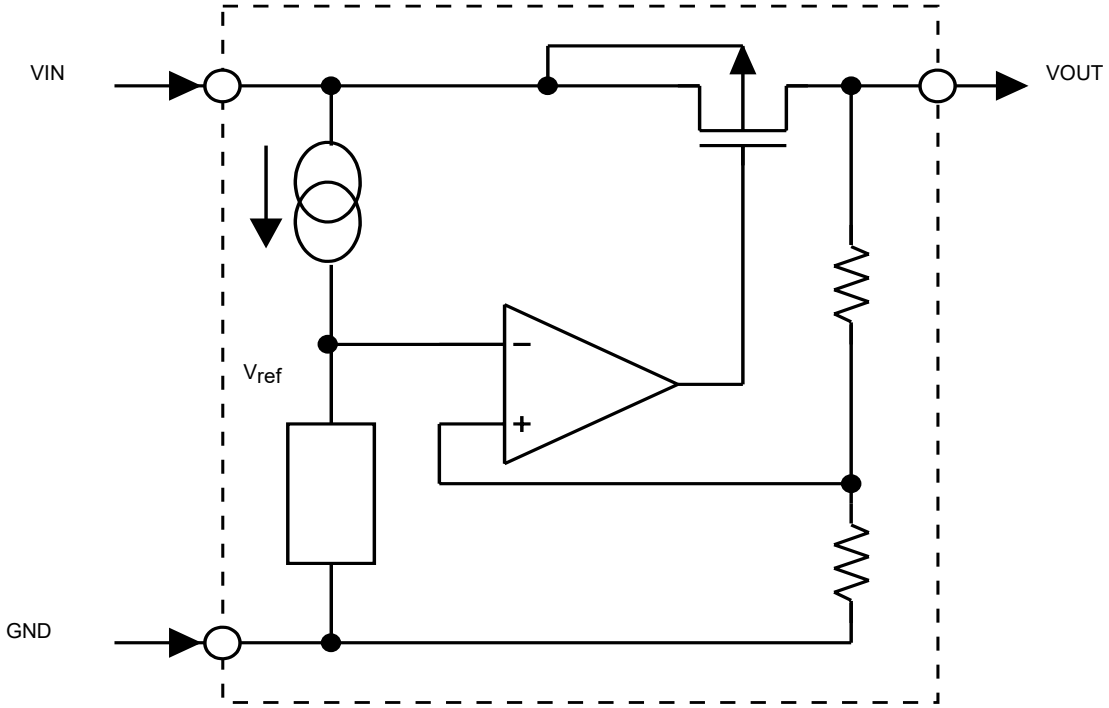
Ordering Information

PJ71□□□□

- Package Type
  SA : SOT-23 SC : SOT-23-3
  SQ : SOT-89
- Output Voltage
  30 : 3.0V 33 : 3.3V 36 : 3.6V
  44 : 4.4V 50 : 5.0V
- Output current tap
  K: 30mA

Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan Note	MSL Level	Marking Code
PJ71K30SA	SOT-23	7	3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 30:3.0V
PJ71K33SA						
PJ71K36SA						
PJ71K44SA						
PJ71K50SA						
PJ71K30SQ	SOT-89	7/13	1000/3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 30:3.0V
PJ71K33SQ						
PJ71K36SQ						
PJ71K44SQ						
PJ71K50SQ						
PJ71K30SC	SOT-23-3	7	3000	RoHS & Green	MSL3	 XX:Output Voltage e.g. 30:3.0V
PJ71K33SC						
PJ71K36SC						
PJ71K44SC						
PJ71K50SC						

Function Block Diagram



Absolute Maximum Ratings

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
Supply Voltage		-0.3 ~ +24	V
Power Dissipation	SOT-23	200	mW
	SOT-23-3	400	mW
	SOT-89	600	mW
Thermal Resistance,Junction-to-Ambient	SOT-23	500	°C/W
	SOT-23-3	300	°C/W
	SOT-89	180	°C/W
Operating Ambient Temperature		-40 ~ +85	°C
Storage temperature range		-65 ~ +125	°C

Electrical Characteristics

(V_{IN}=V_{OUT}+2, C_{IN}=10μF, C_{OUT}=10μF, T_A=25℃ , unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		--	--	24	V
Output Voltage Accuracy	ΔV_{OUT}		-5	--	+5	%
Output Current	I_{OUT}		20	30	--	mA
Quiescent Current	I_Q	I_{OUT}=0mA	--	5	9	μA
Dropout Voltage Note1	V_{DROP}	3.0V≤V_{OUT}≤5.0V, I_{OUT}=1mA	--	100	--	mV
Line Regulation	ΔV_{LINE}	V_{IN}=V_{OUT}+2 to 24V,I_{OUT}=1mA	--	0.2	--	%/V
Load Regulation	ΔV_{LOAD}	V_{IN}=V_{OUT}+2V,1mA<I_{OUT}<30mA	--	60	100	mV

Note 1. The dropout voltage is defined as V_{IN} – V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

Functional Description

Input Capacitor

A 10μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125 ℃, T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.

The power dissipation definition in device is :

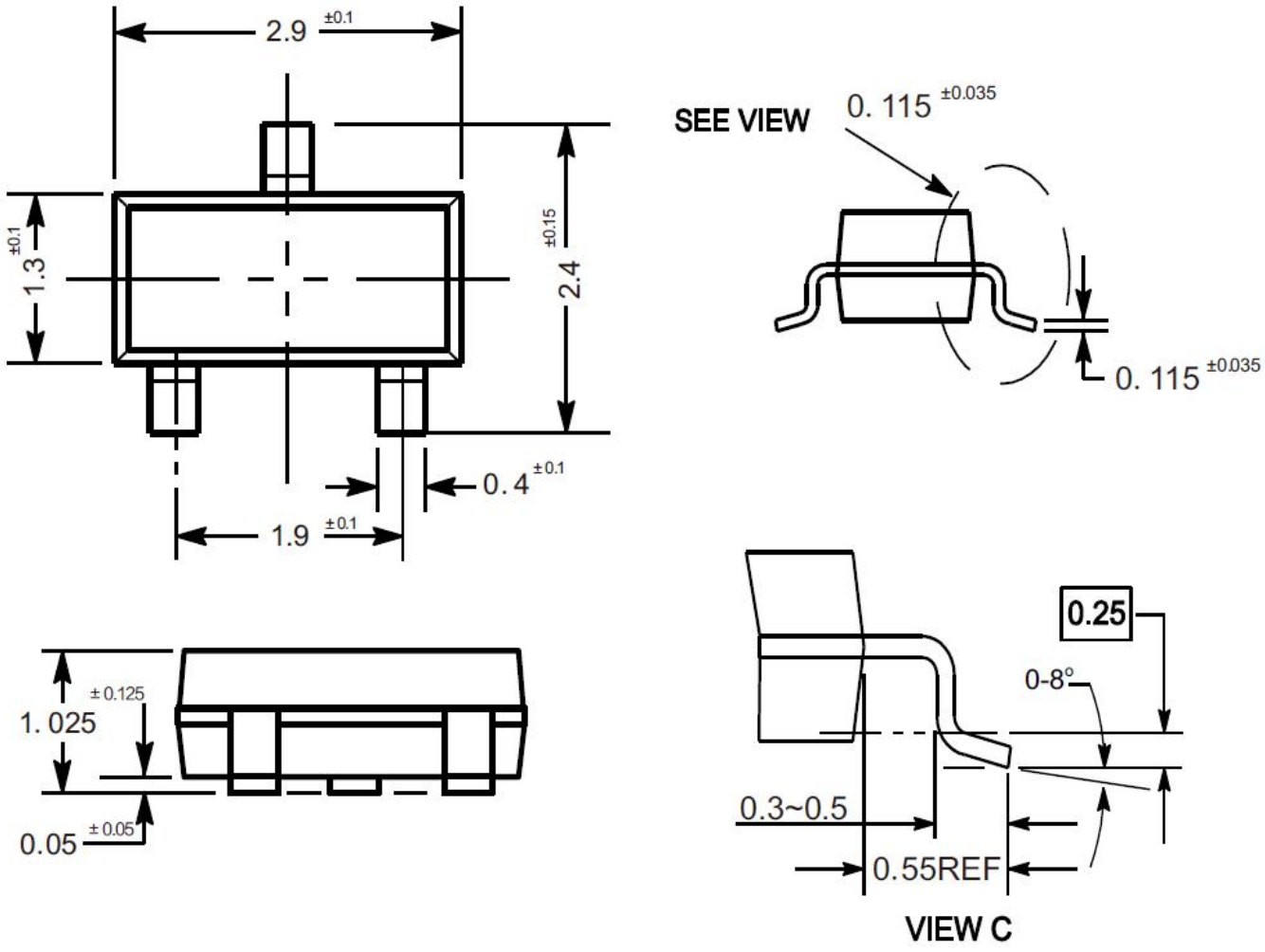
$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the PJ71 Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

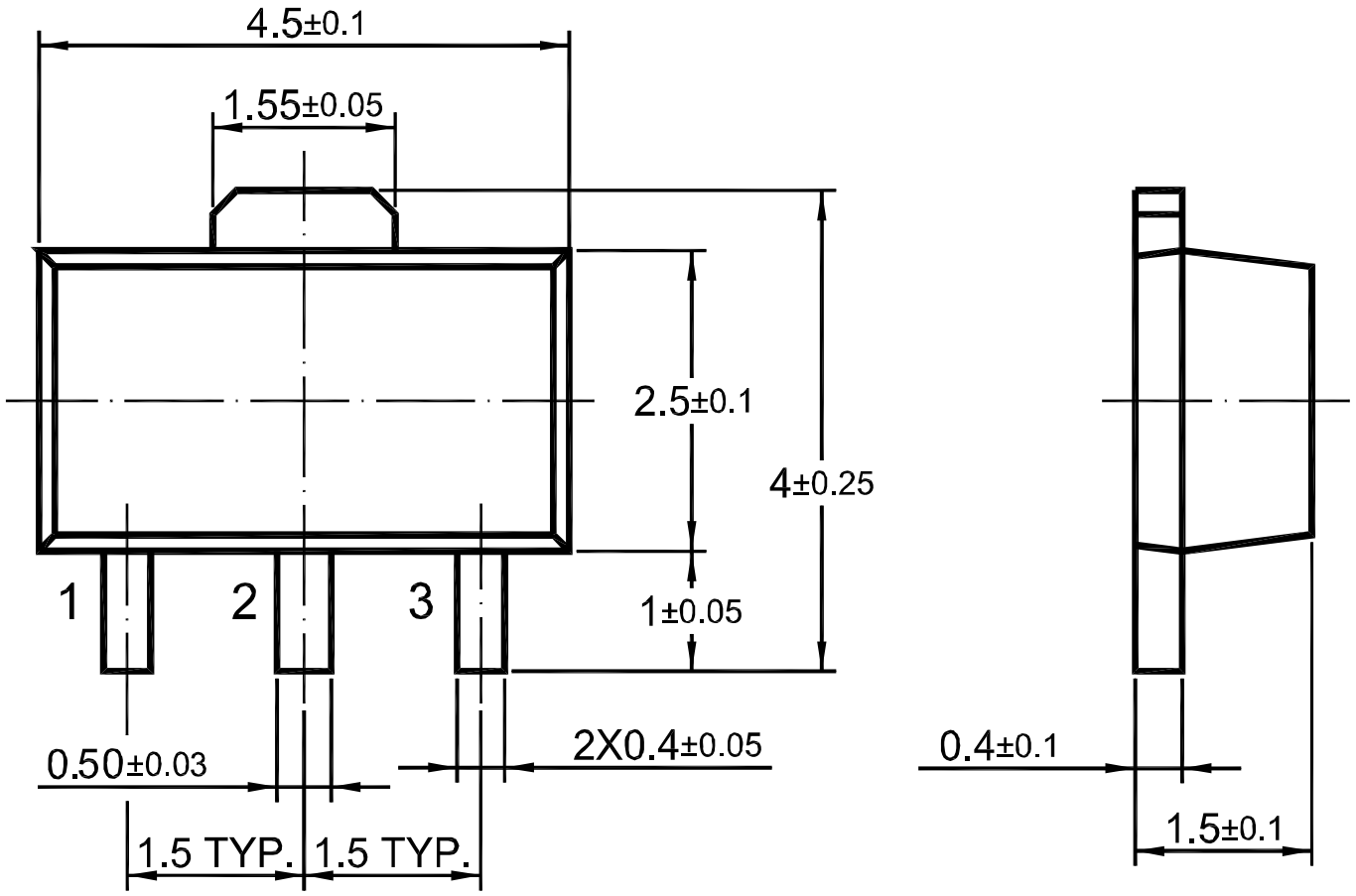
Package Outline

SOT-23
Dimensions in mm



Package Outline

SOT-89
Dimensions in mm



Package Outline

SOT-23-3
Dimensions in mm